IN THE CLAIMS:

Please amend the claims as follows:

1. (Canceled).

2. (Previously presented) An integrated circuit package, comprising:

a semiconductor substrate including a set of semiconductor devices separated by one or more interior scribe lanes; and

an interconnect channel extending across the one or more interior scribe lanes to electrically connect at least two semiconductor devices.

3. (Previously presented) An integrated circuit package, comprising:

a semiconductor substrate including a set of semiconductor devices separated by one or more scribe lanes, where at least one semiconductor device is electrically connected to a device bond pad formed on the semiconductor substrate;

an interconnect substrate positioned on the semiconductor substrate and including a substrate bond pad, wherein a bond wire electrically connects the device bond pad and the substrate bond pad; and

an interconnect channel disposed in the interconnect substrate and extending across the one or more scribe lanes to electrically connect at least two semiconductor devices.

4. (Previously presented) The integrated circuit package of claim 3, wherein the interconnect substrate further includes at least one bond ball for bonding the integrated circuit package to a printed circuit board or other substrate.

5. (Previously presented) The integrated circuit package of claim 3, wherein the interconnect substrate includes flexible tape.

6. (Previously presented) The integrated circuit package of claim 2, wherein the interconnect channel includes metal traces.

7. (Currently amended) An integrated circuit package, comprising:

a semiconductor substrate including a set of semiconductor devices separated by one or more scribe lanes; and

an interconnect channel including an interconnect substrate positioned on the semiconductor substrate ~~and~~, wherein the interconnect channel ~~including~~ includes at least one

via extending through the semiconductor substrate to at least one semiconductor device and electrically connecting the semiconductor device to the interconnect channel[[.]], and wherein the interconnect extends across the one or more interior scribe lanes to electrically connect at least two semiconductor devices.

8. (Previously presented) The integrated circuit package of claim 7, wherein the interconnect channel is electrically connected to a printed circuit board or another substrate.

9. (Previously presented) The integrated circuit package of claim 7, further comprising:

a bus interface for connecting the interconnect channel to an external bus; and

an impedance matching device connected to the bus interface for matching an external bus impedance within a predetermined target range.

10. (Previously presented) The integrated circuit package of claim 7, wherein the interconnect substrate includes flexible tape.

11. (Previously presented) The integrated circuit package of claim 7, wherein the interconnect channel includes metal traces.

12. (Previously presented) A method of interconnecting integrated circuit devices, comprising:

designating a group of functional devices on a wafer;

interconnecting the group of functional devices with an interconnect channel;

defining scribe lanes on the wafer; and

cutting the wafer along selected scribe lanes, so that the grouped functional devices remain interconnected by the interconnect channel.

13. (Previously presented) The method of claim 12, further comprising:

packaging the grouped functional devices into an integrated circuit package.

14. (Previously presented) The method of claim 13, further comprising:

testing the packaged grouped functional devices.

15. (Previously presented) The method of claim 14, further comprising:

applying a bypass to at least one non-functional device in the grouped functional devices.